Digital On-chip Temperature Sensor with I²C Interface

Features

- Temperature accuracy
  - ±1°C(max.) from 0°C~ 100°C
  - ±2°C(max.) from -40°C~ 125°C
- Low power consumption
  - 4.5uA shutdown current at VDD=5.0V
  - 125uA continuous conversion current
- 2.5~5.5V ultra-wide operation supply voltage
- High PSR in temperature monitoring
- I2C & SMBus digital communication interface
- LM75 function and register compatible
- 0.0625°C temperature resolution
- Support up to 8 devices by A0/A1/A2 pin hardware configuration
- OS pin open-drain alert and interrupt multi-function
- OS output polarity configuration
- Embedded one-shot conversion mode
- TRIP mode for Hi TEMP and Lo-TEMP detection

Applications

- Home appliance thermal control
- Server board temperature monitoring
- Thermostat control
- Environmental temperature monitoring
- Electronic equipment and facilities
- General system thermal management

Description

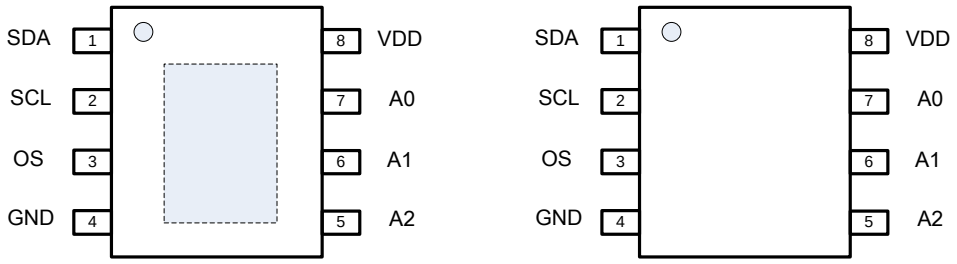
The ETS75A is a digital-type high-accurate on-chip integrated temperature sensor chip with an integrated high-resolution sigma-delta converter and I2C/SMBus digital interface. It is register and function compatible with industrial standard LM75 digital temperature sensor. ETS75A is available in E-MSOP8 package, it offers hardware pin and firmware compatibility to easy upgrade from LM75x design.

Digital communication 2-wire interface which operates up to 400KHz of fast mode. There are 3 hardware address pins, A0/A1/A2, which could configure the I2C address externally.

The ETS75A has a dedicated over-temperature shutdown output (OS) pin with programmable higher or lower limit in hysteresis. The OS pin could also be output polarity reverse by configure POL register bit setting in configuration register.

There is a consecutive fault measurements function which could be programmed by 1/2/3/4 counts. The OS pin will enabled if the temperature conversion data is over the pre-set limitation value continuously, and satisfies the FQ[1:0] resister setting.

Pin Assignments



Pin Description

Pin		I/O	DESCRIPTION
No.	Name		
1	SDA	I/O	I2C data pin
2	SCL	I	I2C clock input pin
3	OS	O	Over-temperature shutdown output (open-drain type)
4	GND	P	Ground terminal
5	A2	I	Device I2C address configuration inputs
6	A1	I	
7	A0	I	
8	VDD	P	Power supply terminal

Ordering Information

Product ID	Package	Packing / MPQ	Comments
ETS75A-MT08NNR	EMSOP-8L	Tape & reel / 3000 Units	Green

Marking Information

Marking Information
Line 1：Product name
Line 2：Date code

Absolute Maximum Ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

PARAMETER	CONDITIONS	MIN	MAX	UNIT
Supply voltage	VDD	-0.3	8.0	V
Input pin voltage	A0, A1, A2	-0.3	8.0	V
Digital interface	SDA, SCL	-0.3	8.0	V
Output pin voltage	OS	-0.3	8.0	V
Operating temperature range		-40	125	°C
Junction temperature		–	150	°C
Storage temperature range		-55	150	°C
Human Body Model		–	±4K	V
Charged Device Model		–	±500	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

(3) Power dissipation and thermal limits must be observed.

Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	MAX	UNIT
VDD	Supply voltage	2.5	5.5	V
T_A	Operating free-air ambient temperature	-40	125	°C

Thermal Information

Package Type	Device No.	θ_{JA}(°C/W)	θ_{JC}(°C/W)	Exposed Thermal Pad
EMSOP-8L	ETS75A	40	10	(Note 1)

Note 1.1: The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is necessary.

Note 1.2: θ_{JA} is simulated on a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The measurement is simulated using the JEDEC51-5 thermal measurement standard.

Note 1.3: θ_{JC} represents the thermal resistance for the heat flow between the chip junction and the package`s top surface. It`s extracted from the simulation data with obtaining a cold plate on the package top.

Electrical Characteristics

- VDD=2.5~5V, at T_A=-40 ~ 125°C, unless otherwise noted

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
VDD	Supply voltage	Normal operation	2.5	—	5.5	V
I_Q	Quiescent supply	RC[1:0]=11	—	125	200	uA
		RC[1:0]=10/01/00	—	105	150	uA
I_{SD}	Shutdown current	VDD=5.0V	—	4.5	—	uA
		VDD=3.3V	—	4.0	—	uA
Temperature Data						
	Temperature range	—	-40	—	125	℃
	Accuracy	0~100℃	—	±0.5	±1	℃
		-40~125℃	—	±1	±2	℃
	Resolution	1LSB	—	0.0625	—	℃
	Repeatability	1LSB	—	0.0625	—	℃
	Conversion Time	RC[1:0]=11	—	220	—	ms
		RC[1:0]=10	—	110	—	
		RC[1:0]=01	—	55	—	
		RC[1:0]=00	—	27.5	—	
	OS mode conversion	OSM=1	—	14.4	—	ms
Digital I/O Interface						
V_{IH}	Input logic high level	A0, A1, A2 SCL, SDA pins	0.7VDD	—	—	V
V_{IL}	Input logic low level	A0, A1, A2 SCL, SDA pins	—	—	0.3VDD	V
I_{LEAK}	Leakage current	A0, A1, A2 SCL, SDA pins	—	—	0.5	uA
V_{OL}	Output logic low level	I_{SINK}= -3mA	—	0.15	0.4	V
		I_{SINK}= -5mA	—	0.2	0.4	V

Timing Specification

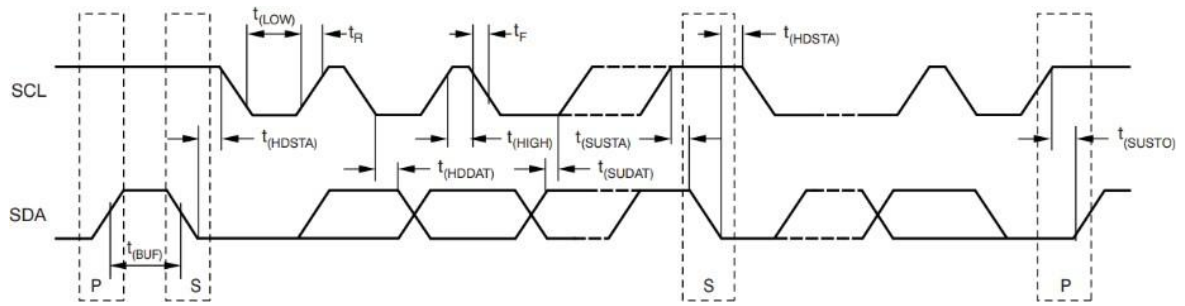
- VDD=2.5V ~ 5.5V, at T_A=25°C (unless otherwise noted) (*1)

SYMBOL	CONDITION	MIN	MAX	UNIT
f_{SCL}	SCL operating frequency	2.5	—	us
f_{BUF}	Bus free time between STOP and START	1.3	—	us
t_{HDSTA}	Hold time after repeated START condition.	600	—	ns
t_{SUSTA}	Repeated START condition setup time	600	—	ns
t_{SUSTO}	STOP condition setup time	600	—	ns
t_{HDDAT}	Data hold time (*2)	0	—	ns
t_{HSUDAT}	Data setup time	100	—	ns
t_{LOW}	SCL clock low period	1300	—	ns
t_{HIGH}	SCL clock high period	600	—	ns
t_{VDAT}	Data valid time (*3)	—	900	ns
t_{FDA}	Data fall time	—	300	ns
t_R	Clock rise time	—	300	ns
t_F	Clock fall time	—	300	ns
Time out	Bus release time out	2	—	ms
$t_{RCClock/data}$	rise time for SCL=100KHz	—	1	us

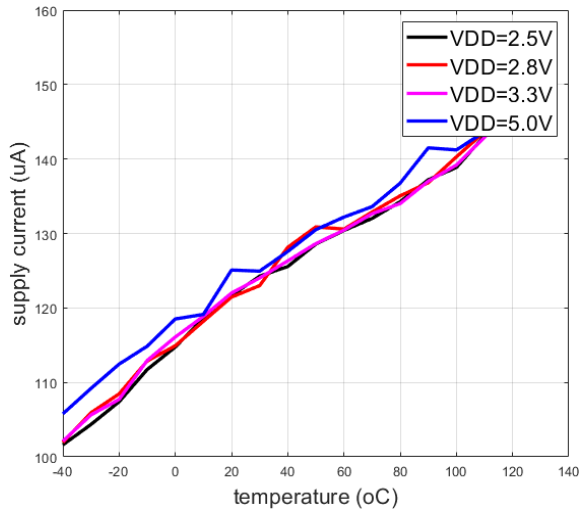
(*1) The host and device have the same VDD voltage. The voltages are based on statistical analysis of samples tested during initial release.

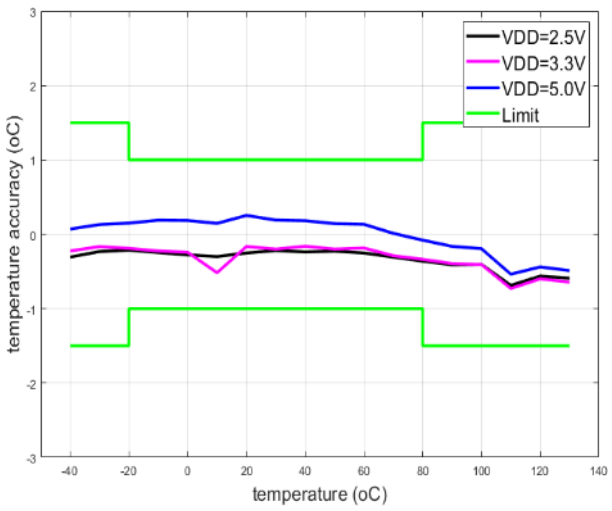
(*2) The maximum t_{HDDAT} can be 0.9us for fast mode, and is less than the maximum t_{VDAT} by a transition time.

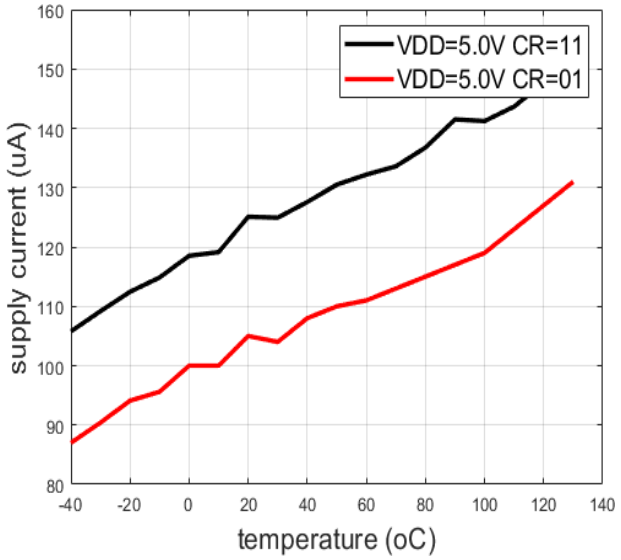
(*3) t_{VDAT}=time for data signal from SCL LOW to SDA output (HIGH to LOW, depending on which is worst). = time for data signal from SCL LOW to SDA output (HIGH to LOW, depending on which is worse).

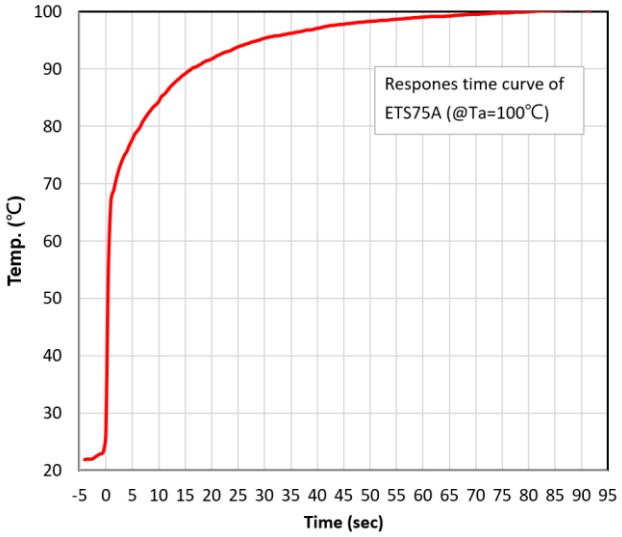


Typical Characteristics









Function Description

Overview

The ETS75A is an on-chip digital temperature sensor which is applicable in environment temperature management and thermal protection. The device is I2C and SMBus interface compatible. The device is specified over a temperature range of -40℃ to 125℃. The Block diagram section shows the functional block diagram of ETS75A device.

The temperature sensor thermal path goes through thermal pad on assembly bottom and package leads as well as the plastic package. The thermal path will run by lowest thermal resistance of the assembly.

Block Diagram

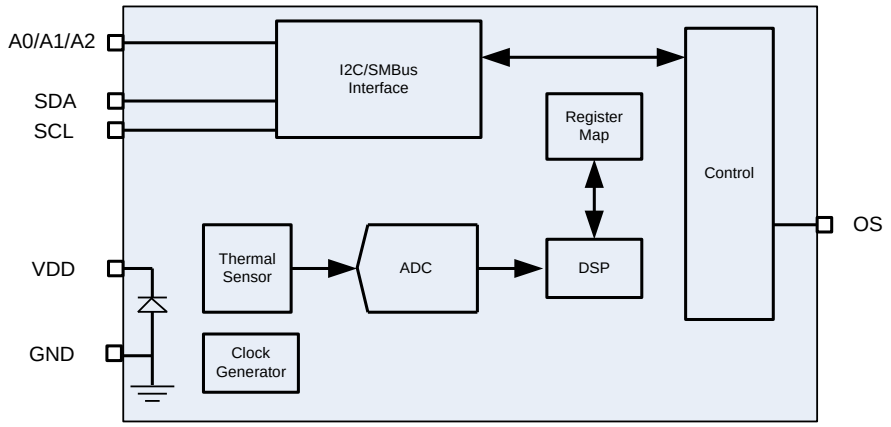


Figure 1. EST75A Block Diagram

Digital Temperature Output

The temperature register saves the temperature measurement data from analog-to-digital converter. The register is read-only and contains two 8-bit data bytes consisting of one Upper Byte and one Lower Byte. However, only the first 12 MSBs are used to store the temperature data in 2's complement format with 0.0625℃ resolutions while the remaining 4 LSB are set to zero. The MSB bit of the upper byte is a sign bit which used to indicate positive or negative data. Table 1 shows the bit arrangement of the temperature data in the dual-byte register.

Upper Byte								Lower Byte							
T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0
sign	64℃	32℃	16℃	8℃	4℃	2℃	1℃	0.5℃	0.25℃	0.125℃	0.0625℃	—	—	—	—

Table 1. Temperature register

Temperature (°K)	Temperature (°C)	Digital Output	
		Hex Value	Binary Value
400.15	127	7F00	0111 1111 0000 0000
373.15	100	6400	0110 0100 0000 0000
353.15	80	5000	0101 0000 0000 0000
348.15	75	4B00	0100 1011 0000 0000
323.15	50	3200	0011 0010 0000 0000
298.15	25	1900	0001 1001 0000 0000
273.4	0.25	0040	0000 0000 0100 0000
273.2125	0.0625	0010	0000 0000 0001 0000
273.15	0	0000	0000 0000 0000 0000
273.0875	-0.0625	FFF0	1111 1111 1111 0000
272.9	-0.25	FFC0	1111 1111 1100 0000
248.15	-25	CE00	1110 0111 0000 0000
233.15	-40	D400	1101 1000 0000 0000

Table 2. Temperature Data Format

Note1：For 9-bit temperature data ism compatible with LM75, just use only 9 MSB bits of the Upper Byte in the two bytes and disregard 7 LSB bits of the Lower Byte. The 9-bit temperature data with 0.5 resolution of the device is defined exactly in the same way as for the standard LM75.

Note2：User could read the required temperature resolution data in specified application even 1°C resolution is allowed.

Note3：The MSB bit of the temperature data is dedicated for Sign-bit to indicate the positive temperature or negative temperature. The temperature data is stored in 2's complement data format.

I2C and SMBus Serial Interface

The ETS75A can be connected to a compatible 2-wire serial interface as a slave device under a controller or master device. Connections to the bus are made through the open-drain I/O line SDA and SCL input pin. External pull-up resistor is needed for each of the two terminals. There are Schmitt triggers at SDA/SCL input signal chain to minimize the effects of signal fluctuations and bus noises. The ETS75A supports the I2C transmission protocol up to 400KHz clock frequency of fast mode.

I2C Bus Overview

The data register in the ETS75A are selected by Pointer register. At power-up, the Pointer Register is set to 0x00. Each data register falls into one of three types of user accessibility, (a) Read Only (b) Write only (c) Write/Read same address.

A write command to this device will always include the address byte and the pointer byte. A write to any register other than the Pointer register requires two data bytes.

Bus Fault Timeout

The ETS75A supports SMBus timeout feature. If the host holds the SCL pin in "L" more than 2ms(typ.) between a START and STOP condition, the ETS75A would reset its internal state machine to prevent a system bus hang-up. This feature is turned on by default and release SDA and waits for a START condition.

Slave Address

To communicate with the ETS75A, the master device must first address devices through a 7-bit device address, a direction bit indicating the intent of executing a read or write operation. The ETS75A features 3 external hardware address pins to allow up to 8 devices to be addressed on a single serial I2C bus interface. Table 3 shows the pin setting can connect up to 8 devices. The A0, A1 and A2 pins are samples on every bus communication and must be set prior to any activity on the interface. The default value at power-up is 0x00.

A2	A1	A0	Slave Address
0	0	0	1001000 (0x48)
0	0	1	1001001 (0x49)
0	1	0	1001010 (0x4A)
0	1	1	1001011 (0x4B)
1	0	0	1001100 (0x4C)
1	0	1	1001101 (0x4D)
1	1	0	1001110 (0x4E)
1	1	1	1001111 (0x4F)

Table 3. Device addresses definition

General Call Reset Function

The ETS75A responds to the two-wire general call address (0000 000) if the LSB bit is 0. The device acknowledges the general call address and responds to commands in the 2nd byte. If the 2nd byte is 0000 0110, the ETS75A resets the internal registers to the power-up reset values.

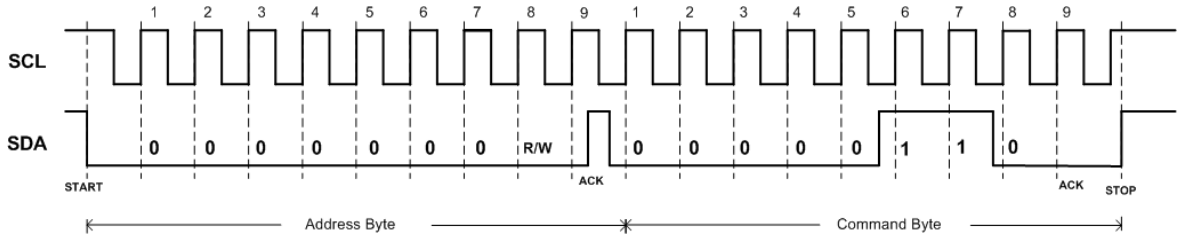


Figure 2. SMBus Timing diagram for General call

SMBus Alert Function

The ETS75A supports the SMBus Alert function. When the ETS75A is operating in interrupt mode, the OS pin of the ETS75A can be connected as a SMBus Alert signal. When the host senses that an alert condition is present on the OS, the host sends a SMBus Alert command on the bus. If the OS pin of the ETS75A is active, the devices acknowledge the SMBus Alert command and respond by returning the device address on the SDA line. The LSB bit of the device address byte indicates if the temperature exceeding T_{HIGH} or falling below T_{LOW} caused the alert condition. This bit is equal to POL if the temperature is greater than or equal to T_{HIGH}. The bit is equal to /POL if the temperature is less than T_{LOW}. The timing diagram shows in Figure 3as below.

If multiple devices on the bus respond to the SMBus OS command, arbitration during the device address portion of the SMBus OS command determines which device clears the alert status. If the ETS75A wins the arbitration, the OS pin becomes inactive at the completion of the SMBus OS command. If the ETS75A loses the arbitration, the OS pin remains active.

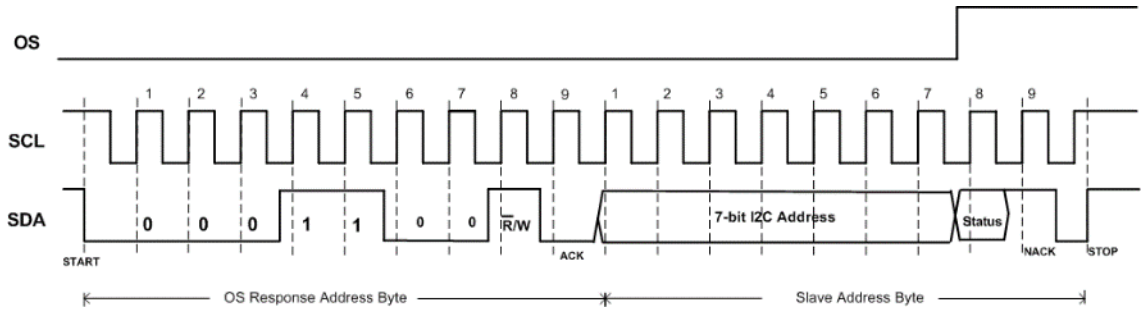


Figure 3. SMBus Timing diagram for OS Function

Timing Diagram

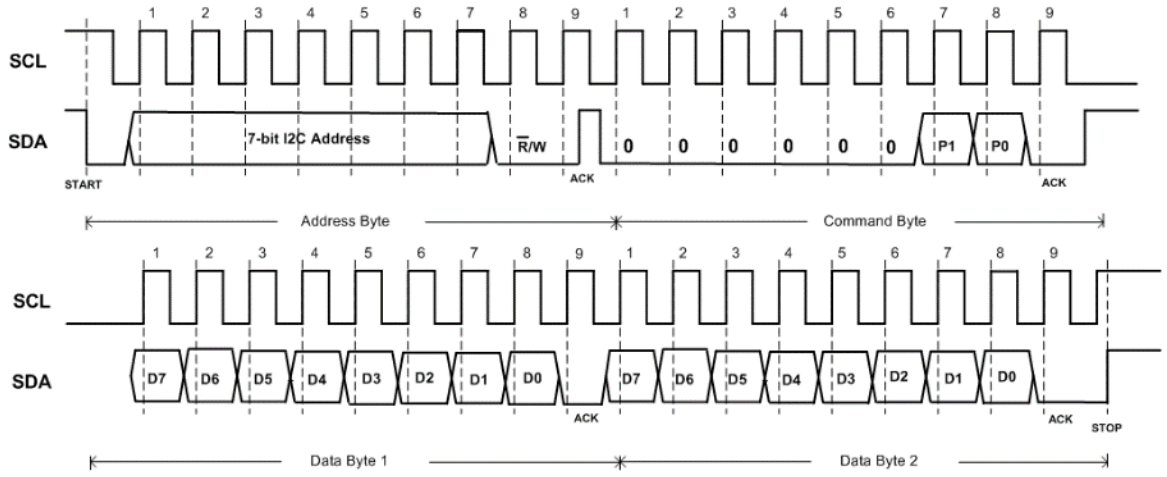


Figure 4. Two-wire timing diagram for Write Two Bytes format

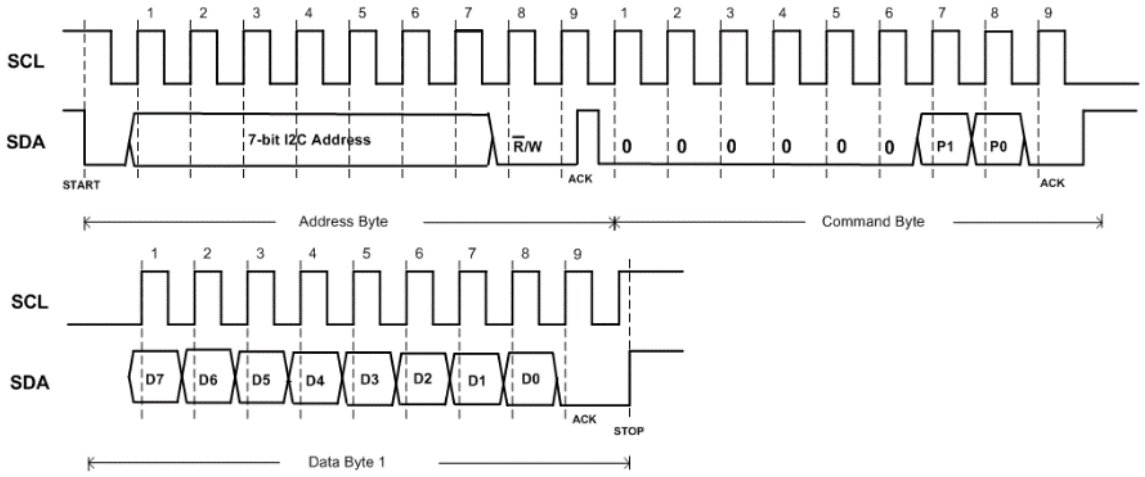


Figure 5. Two-wire timing diagram for Write Single Byte format

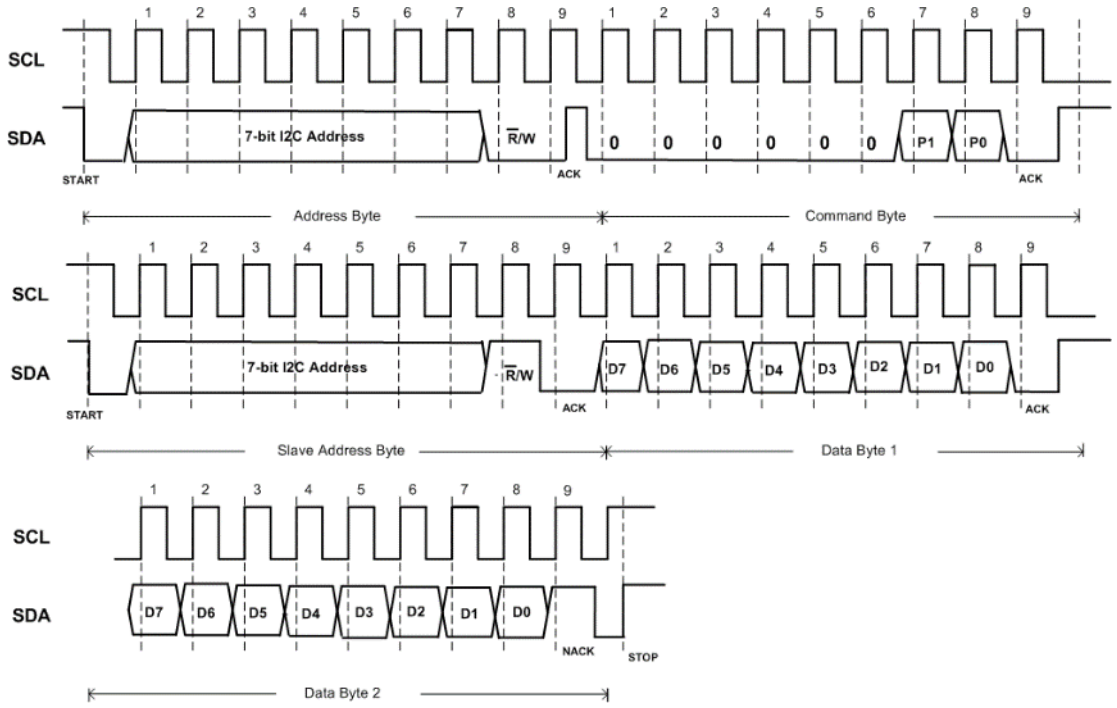


Figure 6. Two-wire timing diagram for Read Two Bytes format

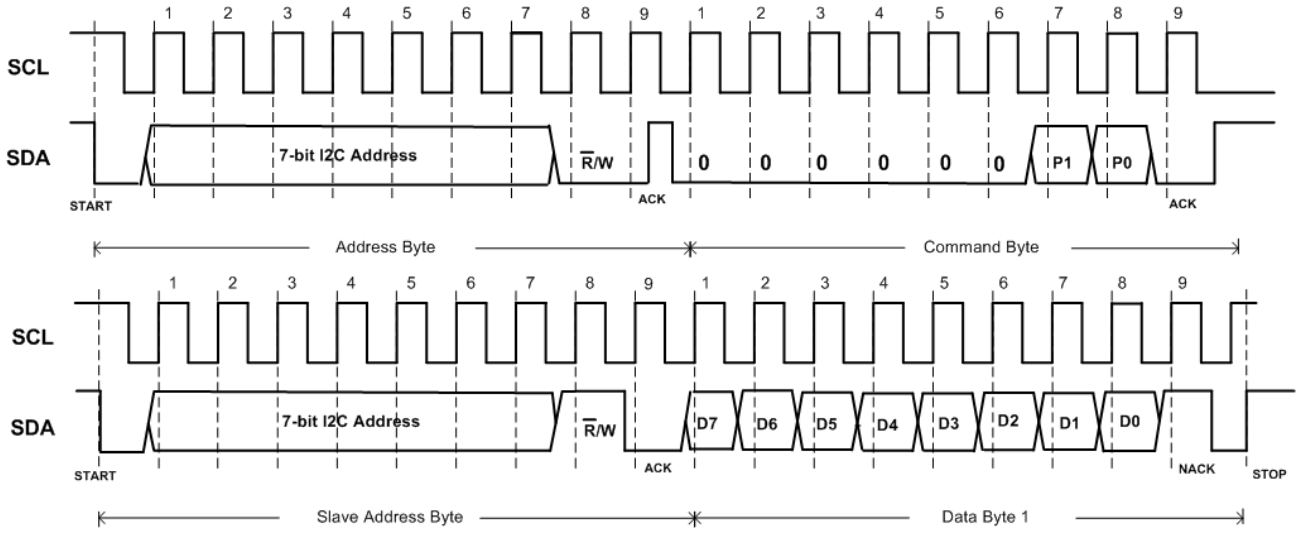


Figure 7. Two-wire timing diagram for Read Single Byte format

Operation Mode

A write to the ETS75A will always include the address byte and the Pointer byte. A write to the Configuration register and limit register requires two data bytes.

Reading the ETS75A can take place in two ways. If the location latched in the Pointer register is correct, then the read can simply consist of an address byte, followed by retrieving the corresponding number of data bytes. If the Pointer register needs to be set, then an address byte, pointer byte, repeat start, and another address byte will accomplish a read. The first data byte is the most significant byte with MSB first, permitting only as much data as necessary to be read to determine temperature condition. At the end of a read, the ETS75A can accept either Acknowledge or No Acknowledge from the master device.

Function Mode

Continuous conversion Mode (CC)

When system power-on, the ETS75A operates in continuous conversion mode. The configuration register initial value is 0x6000. The temperature data will update continuously after every data conversion. The conversion rate is set by RC[1:0] in configuration register. Every conversion cycle consists of an active conversion followed by a standby period.

Shutdown Mode (SD)

The ETS75A can enter shutdown mode if the SD bit in configuration register is set to logic 1. In shutdown mode, all the internal circuit will be disabled and the current consumption will be 4uA (typ.) and the temperature conversion stops. The I2C bus interface remains active and register read/write operation can be performed. When the SD bit is set, the OS output is unchanged in comparator mode and reset in interrupt mode.

One-shot Mode (OS)

One-shot mode should be enabled when ETS75A stays in shutdown mode. User could initiate the one-shot mode before Bit[0]=1 of High-Byte of configuration register. Setting the Bit[7] of High-Byte in Configuration register, OSM, enables the one shot mode. When this mode is enabled, the ETS75A will initiate a temperature conversion once then goes immediately into shutdown mode. After the temperature conversion, the OS pin will be active for master device interruption. The OSM bit will be cleared to logic 0 after a read operation. The temperature conversion will be initiated if the OSM bit setup again. One-shot mode is useful to reduce power consumption in the ETS75A when continuous temperature monitoring is not required.

Thermostat Mode

The thermostat mode can configure the OS pin operates in comparator mode (TM=0) or interruption mode (TM=1). The thermostat mode set by the Bit 1 of Lower Byte of configuration register. Any write to the TM bit will clear the faults count, alert interrupt history and the OS pin will turn to inactive condition.

The main difference between the two modes is that in OS comparator mode, the OS output becomes active when temperature data has exceeded T_{HIGH} and reset when temperature data has dropped below T_{LOW}, reading a register or putting the device into shutdown mode does not change the stat of the OS output. While in interrupt mode, once it has been activated either by exceeding T_{HIGH} or descending below T_{LOW}, the OS output remains

active indefinitely until reading a register, then the OS output will be cleared.

- **Comparator Mode (TM=0)**

  In comparator mode, the OS pin becomes active when the temperature equals or exceeds the T_{HIGH} for a consecutive number of Fault Queue bits FQ[1:0]. The OS pin remains active until the temperature falls below the T_{LOW} value which OS pin toggles back immediately without fault counts. The Fault Queue prevents false alert as a result of system noise.

- **Interrupt Mode (TM=1)**

  In interrupt mode, the device starts to compare temperature readings with the T_{HIGH} register value. The OS pin becomes active when the temperature equals or exceeds T_{HIGH} for a consecutive number conversions which set by FQ[1:0].

  The OS pin condition in interrupt mode will be cleared by 2 conditions, a read of any register, or a successful SMBus Alert response. After the OS pin is cleared, the device starts to compare temperature readings with the T_{LOW}. As the same, the OS pin will active again only when the temperature drops below T_{LOW}.

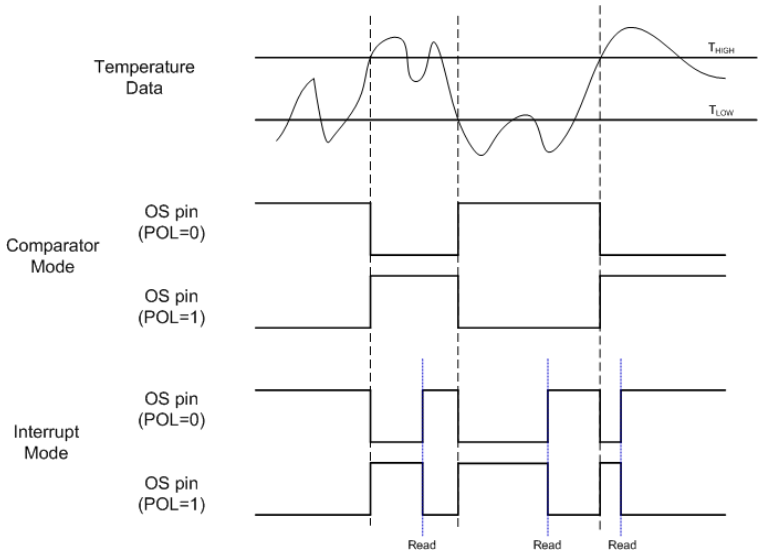


Figure 8. OS pin output transfer function in Interrupt mode and comparator mode (T_TRIP=0)

- **TRIP Mode (T_TRIP=1)**

  In temperature trip mode, OS acts as temperature alert function which is reverse from T_TRIP=0. In TRIP mode, there are comparator mode and interrupt mode as T_TRIP=0.

  In comparator mode, when the environment temperature decrease under the T_{LOW} limit value, and counts to FQ[1:0] times, the OS pin will active Low to alert system. If the temperature ramps up equal to or exceeds T_{HIGH} limit value, the OS pin will release the alert signal and return to High level.

  In interrupt mode, the device starts to compare temperature readings with the T_{LOW} register value. The OS pin becomes active when the temperature equals or drops below T_{LOW} for a consecutive number

conversions which set by FQ[1:0]. The OS pin condition in interrupt mode when T_TRIP=1 will be cleared by 2 conditions. In cases of a reading of any register, or a successful SMBus Alert response will release the OS pin in interrupt mode. After the OS pin is cleared, the device starts to compare temperature readings with the T_{HIGH}. If the temperature rises equal to or exceeds THIGH limit value, the OS pin will release the alert signal and return to High level.

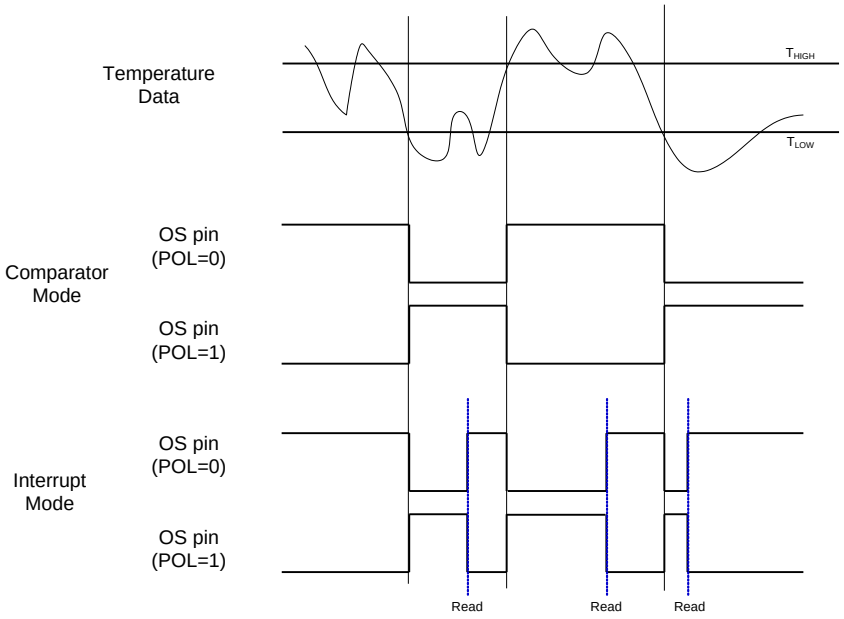


Figure 9. OS pin output transfer function in Interrupt mode and comparator mode (T_TRIP=1)

OS pin output and polarity

The OS pin is an open-drain output and its state represents results of the device watchdog operation. In order to observe this output state, an external pull-up resistor is needed. The resistor should be as large as possible to minimize the temperature data reading error due to internal heating by higher sinking current on OS pin.

The default state of OS pin is active low. If the Bit[2] in Lower byte of configuration register set to 1, the OS pin operation state will change to active high. At power-up, Bit POL will reset to logic0 and the OS pin active state is LOW.

Fault Queue

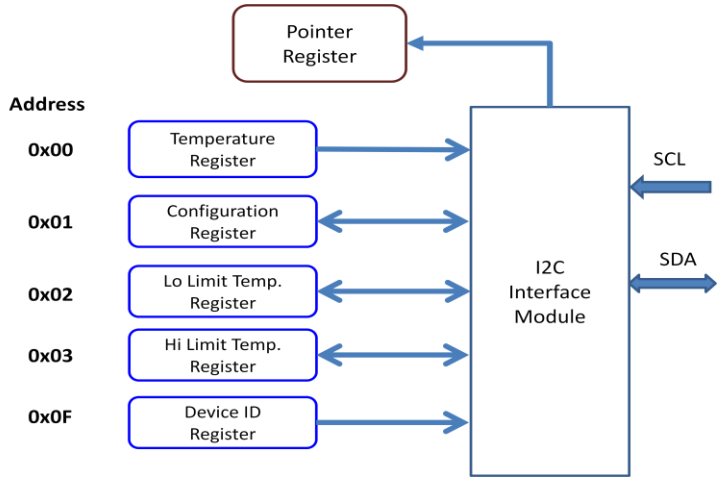
The fault queue value can be programmed in FQ[1:0] in configuration register. Fault queue defines the number of faults that must occur consecutively to activate the OS output. It prevents from false tripping due to system noise or temperature fluctuation. Table XX shows the relationship between register set data and fault queue values.

FQ[1:0]		Fault queue value
0	0	1
0	1	2
1	0	3
1	1	4

Table 4. Fault Queue Configuration

Pointer Register

The following diagram shows the internal register structure of ETS75A. There are 4 data registers and 1 device ID register in ETS75A. The pointer address, read/write capability and reset default value at power-up are shown in Table 5. The pointer register at power-up is set to 0x00. The Temperature register and Device ID register are Read-only, others are Read/Write capability. In interrupt mode, a read from the ETS75A, or placing the device in shutdown mode, the OS pin output will be reset.



Default	P7	P6	P5	P4	P3	P2	P1	P0
0x00	0	0	0	0	0	0	Register bits	

P1	P0	Register Description
0	0	Temperature (Read Only) ----------Default
0	1	Configuration (Read/Write)
1	0	Lower limit temperature setting
1	1	Higher limit temperature setting

Table 5. Pointer Register Address

Register Map

The ETS75A supports single-byte and two-byte read/write operation by digital serial interface. It is software compatible with industrial standard LM75 devices

ADDR	Name	Length	R/W	Default	B7	B6	B5	B4	B3	B2	B1	B0
0x00	TEMP Register	2 Bytes	R Only	0x0000	TEMP[15:8]							
					TEMP[7:4]				0	0	0	0
0x01	Config. Register	2 Bytes	R/W	0x6000	OSM	RC[1:0]		FQ[1:0]		POL	TM	SD
												T_TRIP
0x02	L-Limit Register	2 Bytes	R/W	0x4B00	TL[15:8]							
					TL[7:4]				—	—	—	—
0x03	H-Limit Register	2 Bytes	R/W	0x5000	TH[15:8]							
					TH[7:4]				—	—	—	—

Table 6. Register Mapping Definition

Temperature Register

The Temperature Register is a 12-bit read-only register. The data is represented by 12-bit 2's complement format, the MSB of the Upper byte is a sign-bit. The first MSB 12 bits indicate the junction temperature conversion data and the last 4 LSB bits equal to 0. The Temperature Register default value is 0x00 at power-up.

Address	W/R		Default	B7	B6	B5	B4	B3	B2	B1	B0
0x00	R-Only	U Byte	0x00	TEMP[15:8]							
		L Byte	0x00	TEMP[7:4]				0	0	0	0

Table 7. Temperature Register

Configuration Register

The Configuration Register is a 16-bit read/write register used to control the operation mode of temperature sensor device. Read and Write operation are performed MSB first. The default value of Configuration Register is 0x6000.

Address	W/R		Default	B7	B6	B5	B4	B3	B2	B1	B0
0x01	R-Only	U Byte	0x60	OSM	RC[1:0]		FQ[1:0]		POL	TM	SD
		L Byte	0x00	0	0	0	0	0	0	0	T_TRIP

Table 8. Configuration Register

Low Limit Temperature Register

Low Limit Temperature Register is a 12-bit read/write register. The data is represented by 12-bit 2's complement format. The default value of the low limit temperature register at power-up is 0x4B00.

Address	W/R		Default	B7	B6	B5	B4	B3	B2	B1	B0
0x02	W/R	U Byte	0x4B	TL[15:8]							
		L Byte	0x00	TL[7:4]				—	—	—	—

Table 9. Low Limit Temperature Register

High Limit Temperature Register

High Limit Temperature Register is a 12-bit read/write register. The data is represented by 12-bit 2's complement format. The default value of the high limit temperature register at power-up is 0x5000.

Address	W/R		Default	B7	B6	B5	B4	B3	B2	B1	B0
0x03	W/R	U Byte	0x50	TU[15:8]							
		L Byte	0x00	TU[7:4]				—	—	—	—

Table 10. High Limit Temperature Register

Application Circuits

The ETS75A is a temperature sensor IC which monitors the PCB or environment temperature of the location where user mounts the device. The A2, A1 and A0 pins could connect up to 8 devices on the same I2C serial bus interface. SDA and SCL is a standard I2C and SMBus protocol in open-drain output with external pull-up resistors. The OS pin will interrupt or alarm master device if the monitoring temperature data over or under the pre-set limit value. The OS pin is an open-drain output with external pull-up resistor. The pull-up resistor design should be tradeoff by speed and power consumption requirements.

A 0.1uF bypass capacitor places between VDD and GND is required for power supply noise filtering, see Figure 11.

The SDA, SCL and OS pin should pull-up to a voltage which could be higher than VDD of ETS75A. If the OS pin is not used, it can either be connected to GND or left floating.

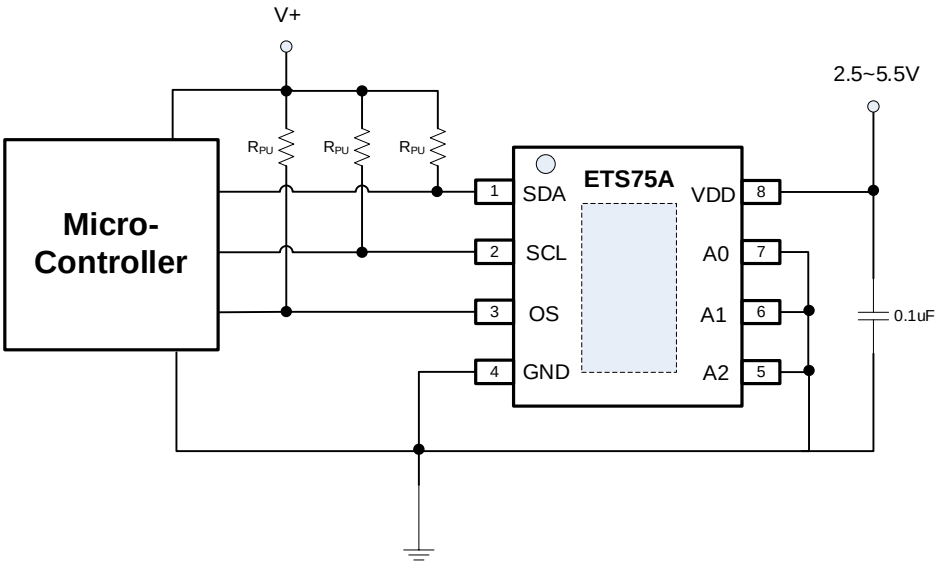


Figure 10. ETS75A Application Circuit 1

The ETS75A is designed to be pin-2-pin and functional compatible with industrial standard LM75 family. The two bytes register of the ETS75A dynamically support single byte read or write operation, meaning that it is software compatible with LM75 devices without any firmware updates.

The ETS75A is a temperature sensor device which monitors the environment temperature. The temperature runs through leads and pads under assembly into silicon junction by thermal conduction. The best device placement ensures that temperature changes are captured within the shortest path and time by junction of temperature sensor. A thermally-conductive adhesive is helpful in achieving accurate surface temperature measurement, see Figure 11.

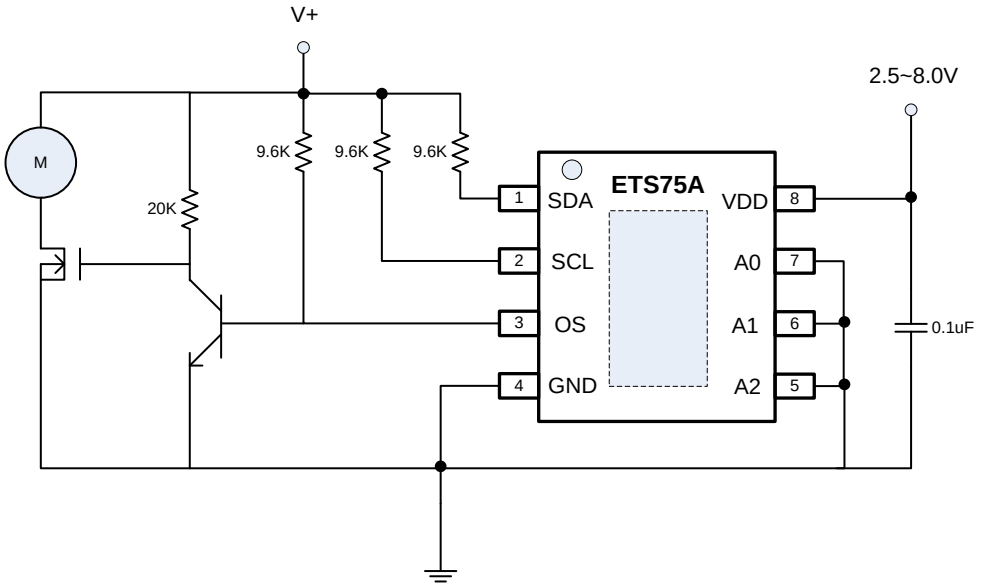


Figure 11. ETS75A Application Circuit 2

The open-drain pull-up resistor could be designed by output driving capability. The minimum pull-up resistor is defined by the sinking current and the maximum output level in equation 1, where VOL (max.) is the maximum logic output low level and IOL is the output sinking current.

$$Rpu(min) = \frac{VDD - V_{OL}(max)}{I_{OL}} \quad \text{(1)}$$

The maximum pull-up resistor is limited by the parasitic capacitance (Cp) and rising time specification of I2C specification. The simplified deduction list in equation 2, where the V_{IL} is 30% of VDD and V_{IH} is defined in 70% of VDD.

$$Rpu(max) = \frac{T_{RISE}}{0.85 * Cp} \quad \text{(2)}$$

Trise is the rising time of signal waveform from 10% to 90% signal full swing. In I2C specification, the rise time of SDA and SCL signals are specified in different value by different operation mode. For example, in standard mode, the maximum rising time is 1000ns. In high speed mode, if the capacitive load from 10pF to 100pF, the rising time specified in 10ns (min.) and 40ns (max.). If the capacitive load is up to 400pF, the rising time is defined in 20ns (min.) and 80ns (max.).

User could design the pull-up resistor by system requirements, also to compliant to the I2C bus operation mode. One thing needs to be reminded that SDA pin is an open-drain output and SCL is a buffer input.

Layout Guidelines

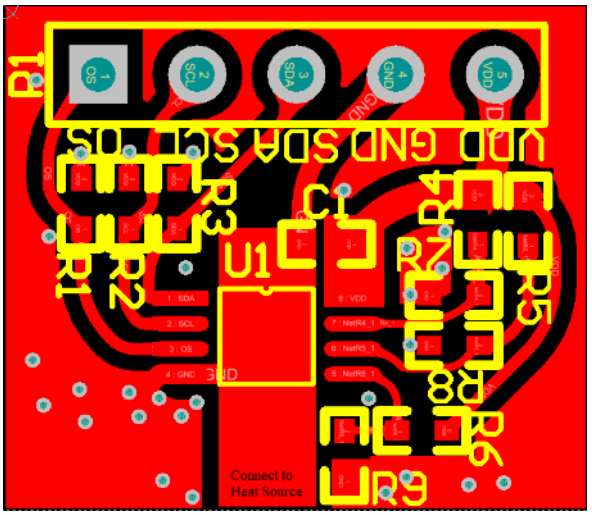


Figure 12. ETS75A EVB Top View

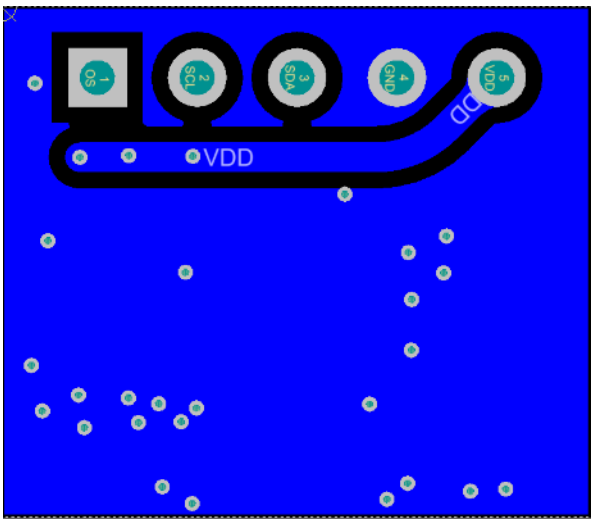
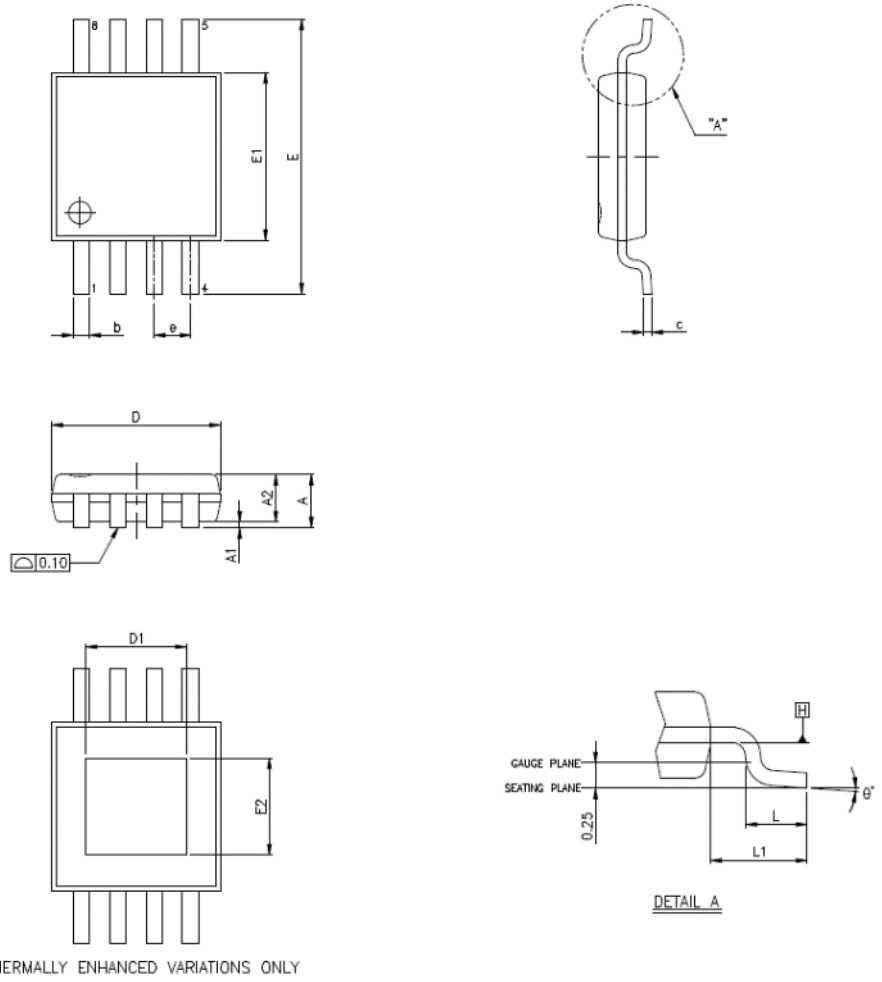


Figure 13. ETS75A EVB Bottom View

Package Dimensions

EMSOP-8L(118mil)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.10
A1	0.00	–	0.15
A2	0.75	0.85	0.95
b	0.22	–	0.38
c	0.08	–	0.23
D		3.00 BSC	
E		4.90 BSC	
E1		3.00 BSC	
e		0.65 BSC	
L	0.40	0.60	0.80
L1		0.95 REF	
θ°	0	–	8

UNIT : MM

Revision History

Revision	Date	Description
1.0	2022.10.07	Original
1.1	2023.01.04	1. Modified Feature item(p1) 2. Modified Description character (p1) 3. Changed Ordering Information table (p2) 4. Modified Electrical Characteristics table voltage condition (p4) 5. Modified Timing Specification table(p5) 6. Added Typical Characteristics figure (p6) 7. Modified note description in Table2. (p8) 8. Modified Operation Mode description (p13~p16) 9. Modified Figure10.(p18) 10. Other misspelling modified and value synchronized in description
1.2	2024.05.29	1. Support up to 8~~(32)~~ devices by pin A0/A1/A2 hardware configuration (p1)(p9)(p18) 2. Table.3 Slave Address from 0x48 to 0x4F (p9)

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